



FUI'19

Waruna project

3rd plenary meeting

Introduction

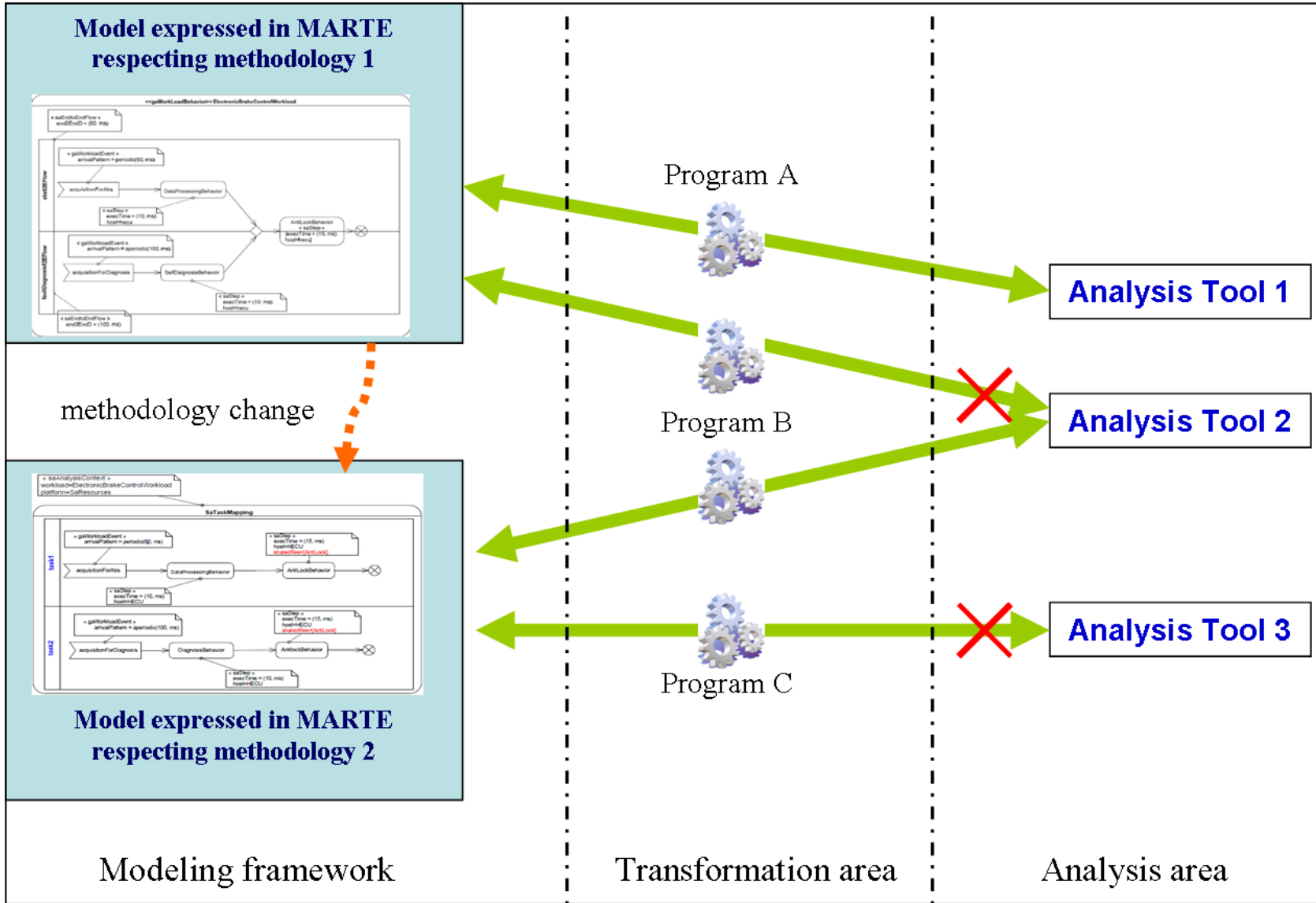
Nicolas Ayache

2019-01-29

Paris
Lyon
Aix
Strasbourg

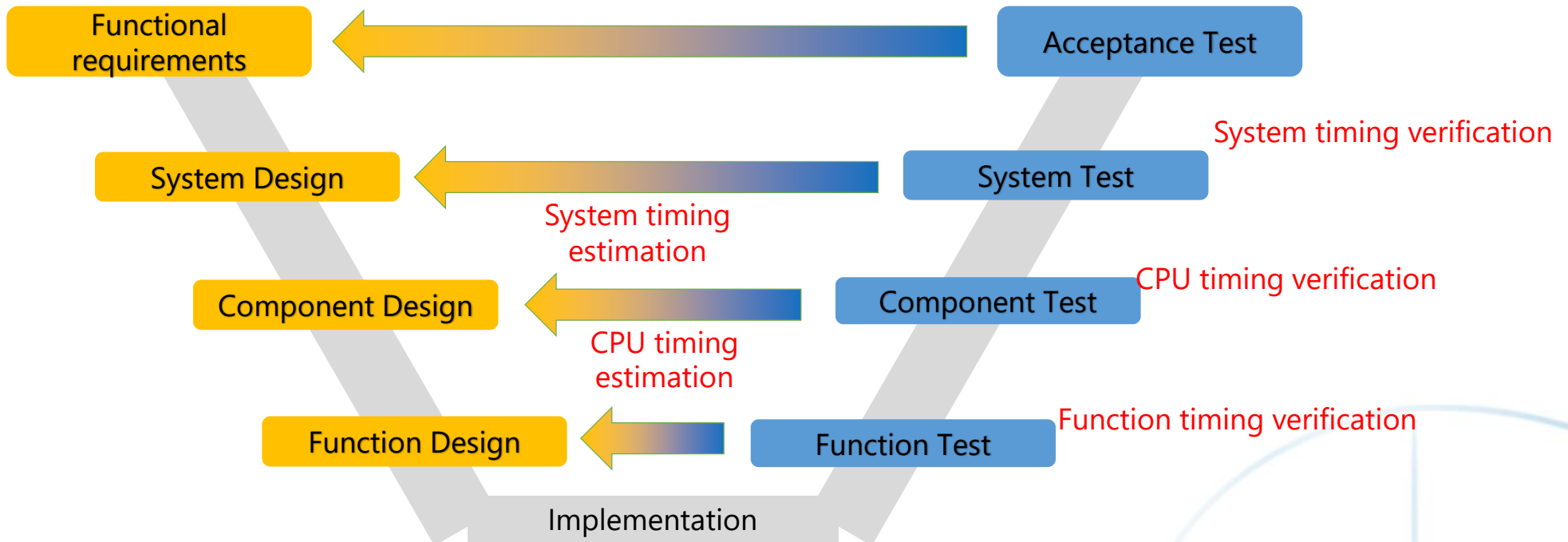


Context





Need for a complete framework from models to timing verifications



Place of **timing analysis** in V-cycle for critical embedded systems



Goals



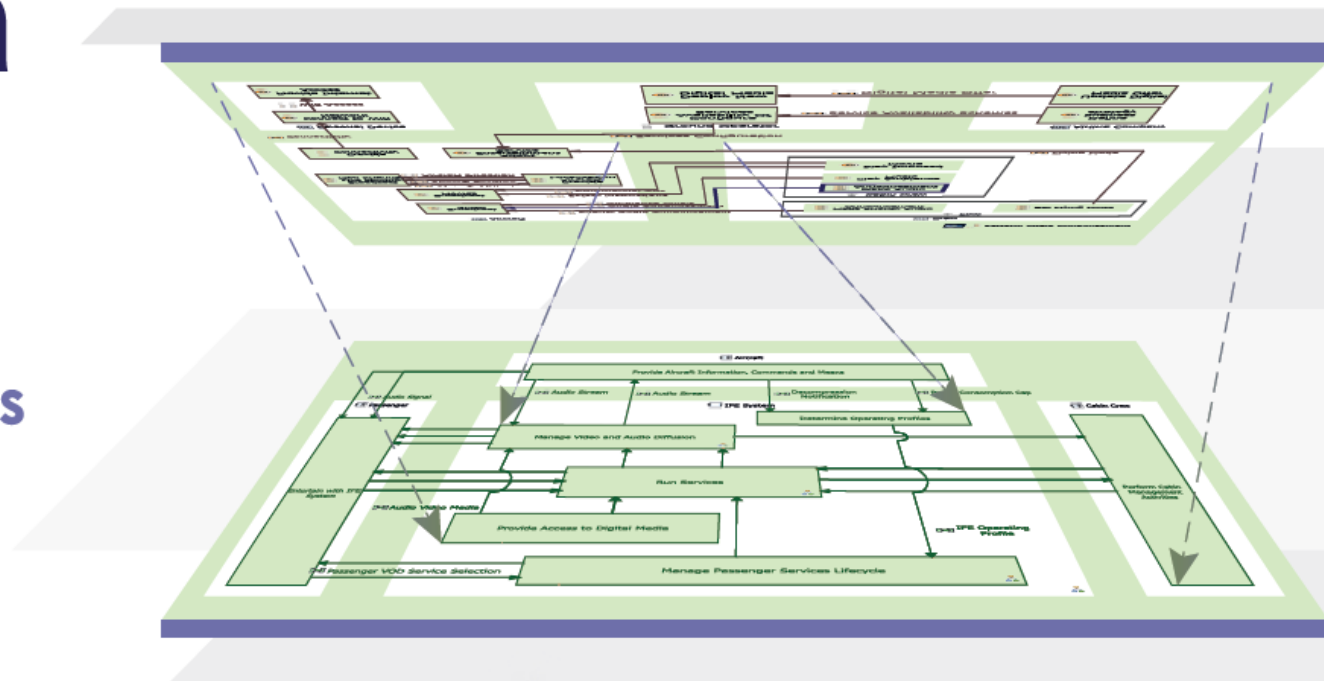
Capella

System Engineering methodology support

from Operational Analysis to Physical Architecture.

Powerful authoring tools.

Design the system architecture





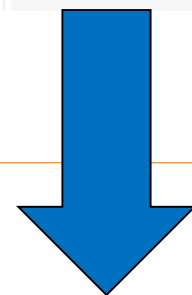
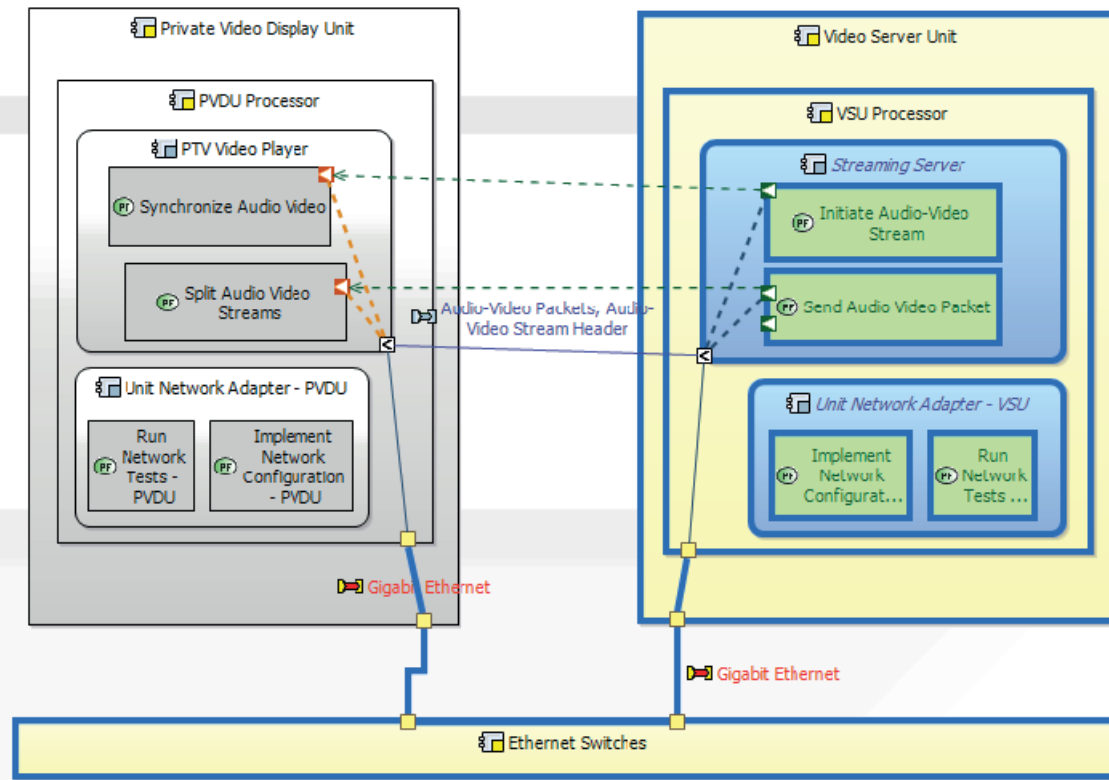
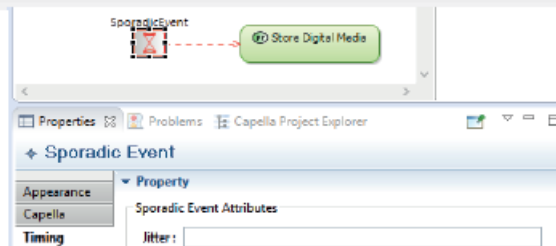
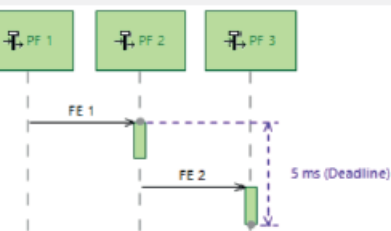
Goals



Tideal

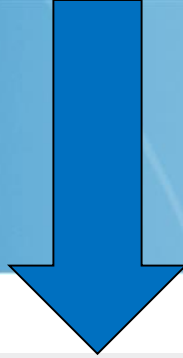
The viewpoint to find the perfect timing

Capella Model with Real Time properties & Constraints



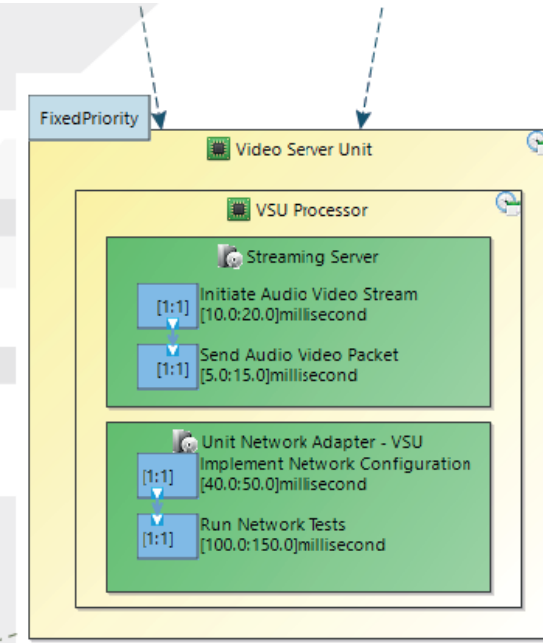
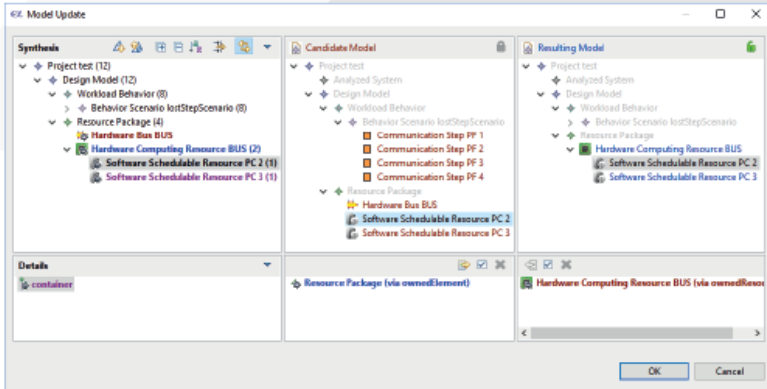


Goals

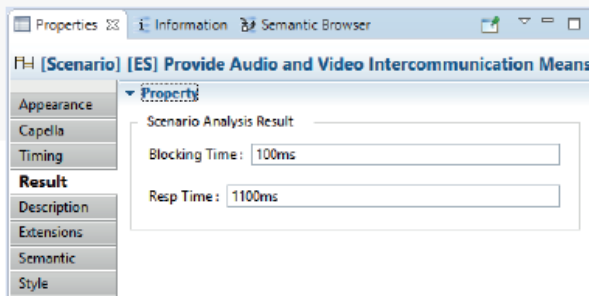


Time4Sys

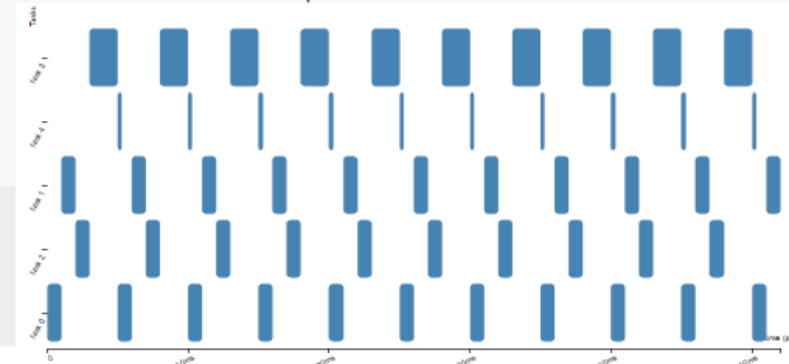
Iterative transformations



Analysis

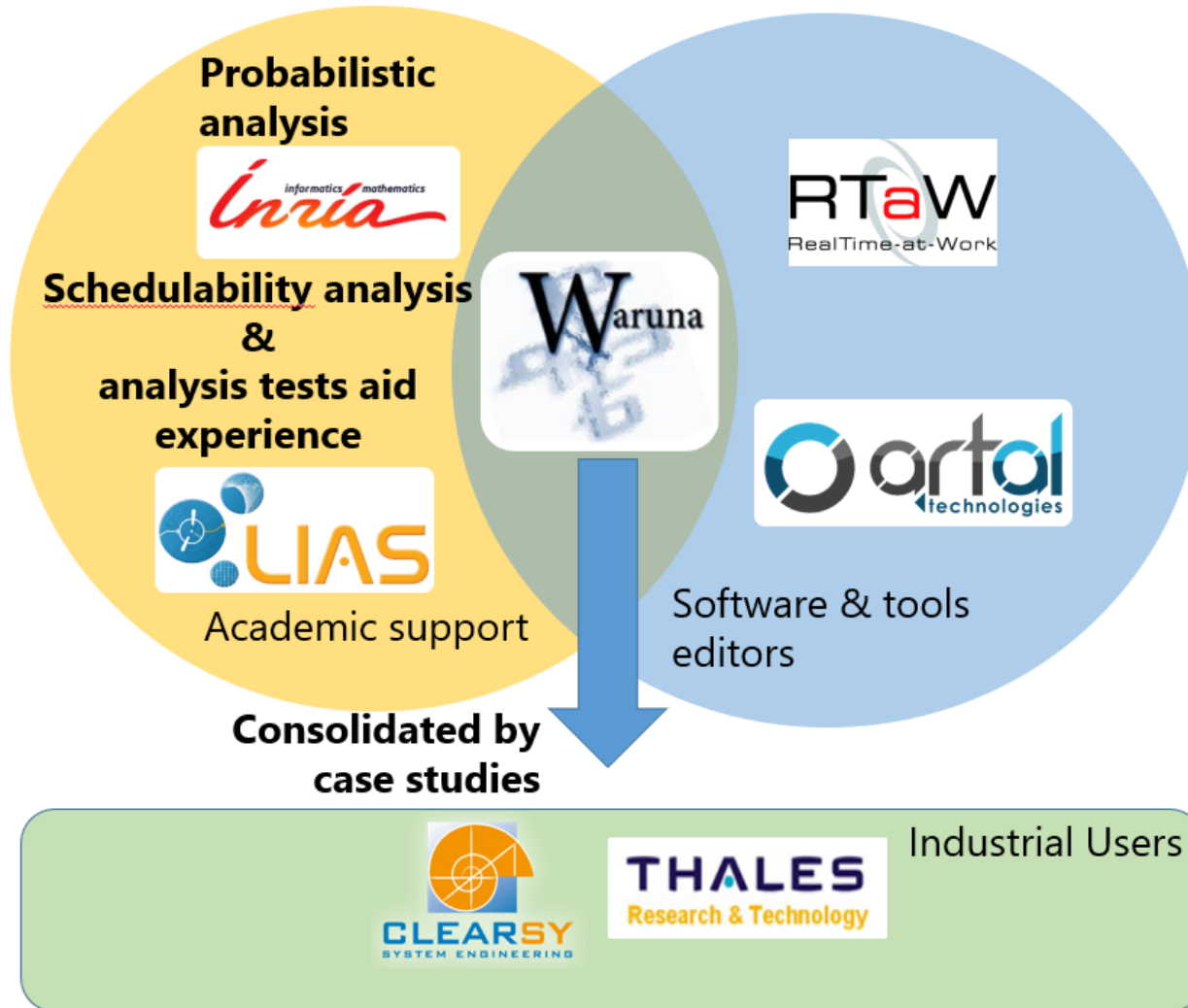


Simulation





Partners



Clusters



Financial support





▶ Agenda



- ▷ Introduction 15 minutes
 - ▶ Nicolas Ayache – ClearSy

- ▷ Scientific contributions: Time4Sys 20 minutes
 - ▶ Emmanuel Grolleau – ENSMA-LIAS

- ▷ Industrial contributions: user environment 20 minutes
 - ▶ Aurélien Didier, Benoit Viaud – Artal Technologies

- ▷ Break 10 minutes

- ▷ Case study 20 minutes
 - ▶ Rafik Henia, Laurent Rioux – Thalès Research & Technology

- ▷ Conclusion 20 minutes
 - ▶ Nicolas Ayache – ClearSy